ABSTRACT OF THE DISCLOSURE

A method and apparatus within a processing system is provided for associating shadow register sets with interrupt routines. The invention includes a vector generator that receives interrupts, and generates exception vectors to call interrupt routines that correspond to the interrupts. The exception vector considers the type of interrupt and the priority level of the interrupt when selecting the exception vector. Shadow set mapping logic is coupled to the vector generator. The mapping logic contains a number of fields that correspond to the different exception vectors that may be generated. The fields are programmable by kernel mode instructions, and contain data mapping each field to one of a number of shadow register sets. When an interrupt occurs, the vector generator generates a corresponding exception vector. In addition, the shadow set mapping logic looks at the field corresponding to the exception vector, and retrieves the data stored therein. The data is used to switch to one of the shadow register sets for use by an interrupt routine. Upon return from the interrupt routine, the previously used register set is selected.